Understanding Heterogeneous Systems Through Topology-Aware Tools

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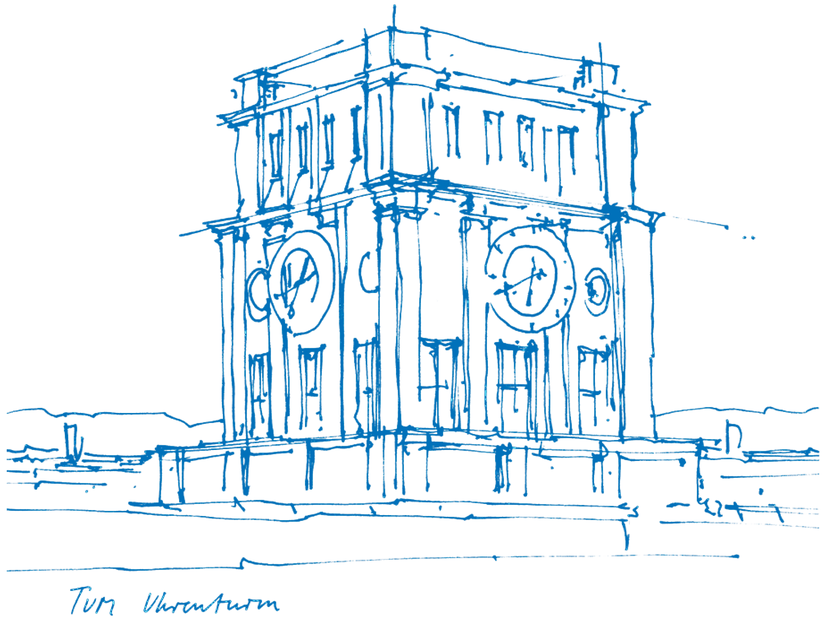

Motivation

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1. Systems are increasingly complex
   - Heterogeneous
   - Dynamic, configurable

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1 Systems are increasingly complex

- Heterogeneous
- Dynamic, configurable

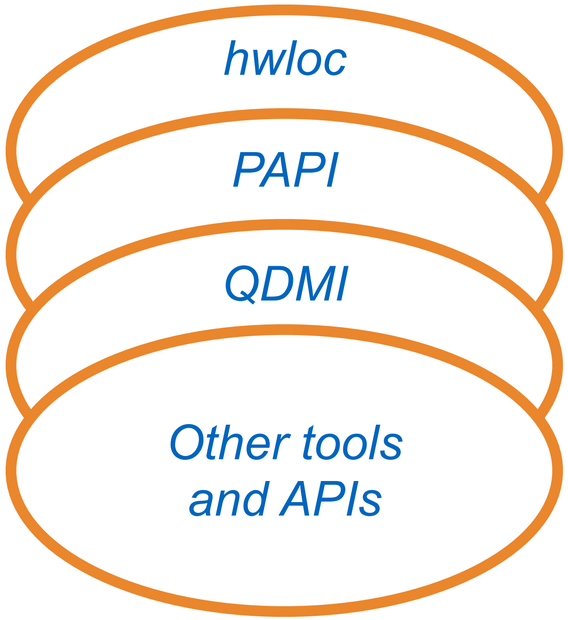
2 Memories play a crucial role

- More parallelism in compute
  - ➡ Higher demand for data
- More complex memory hierarchies
  - ➡ More difficult to understand and tune performance
- More heterogeneous systems, chips, memories
  - ➡ Portability issues

Toolchain Overview

Toolchain Overview

Providing
topology
information



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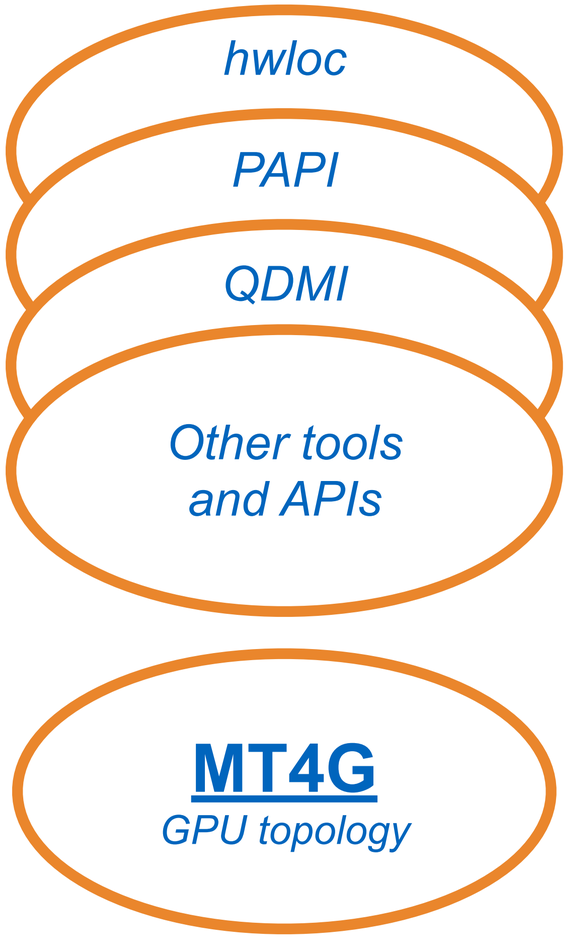

Toolchain Overview

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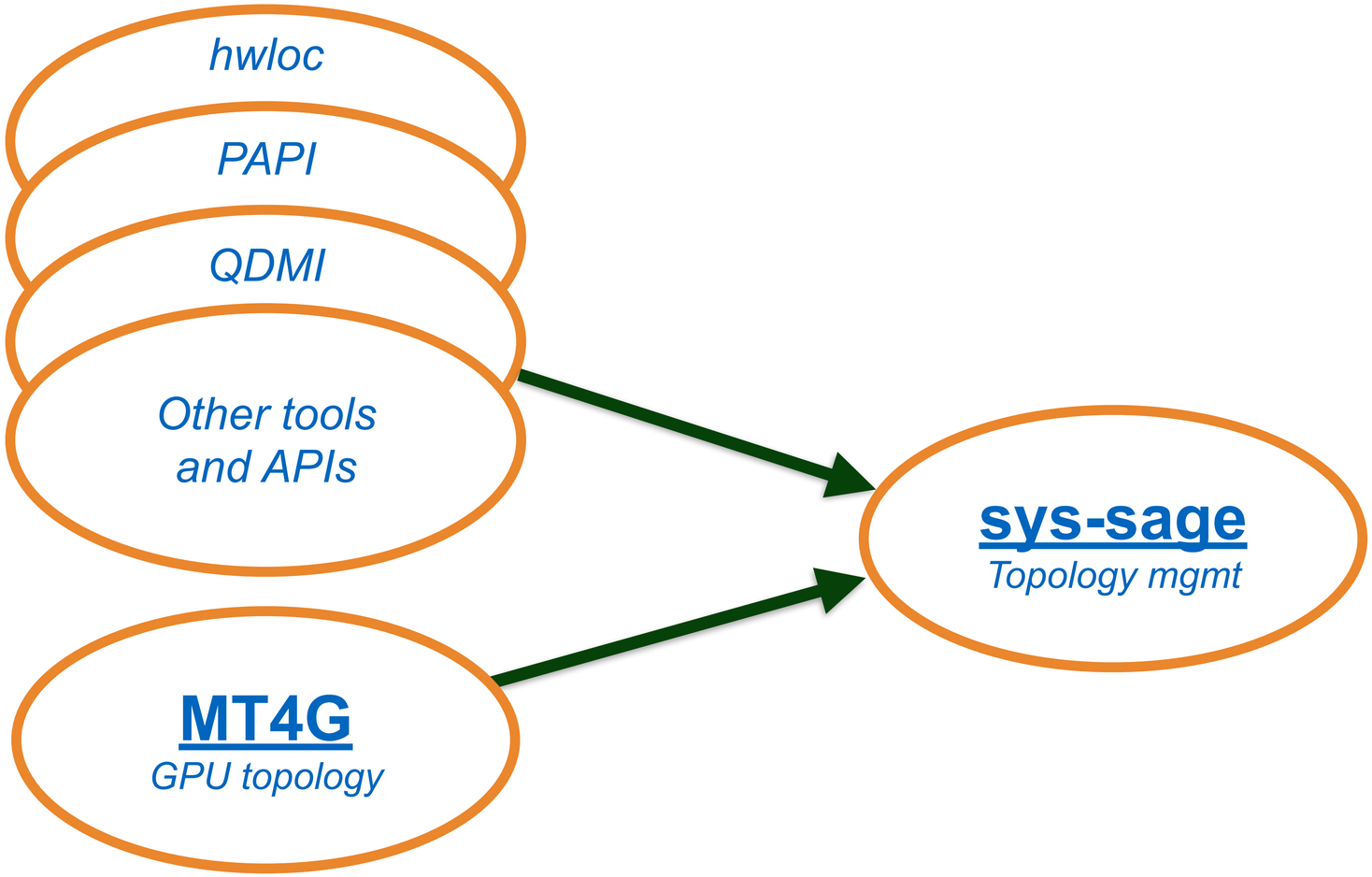

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Managing
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Utilizing
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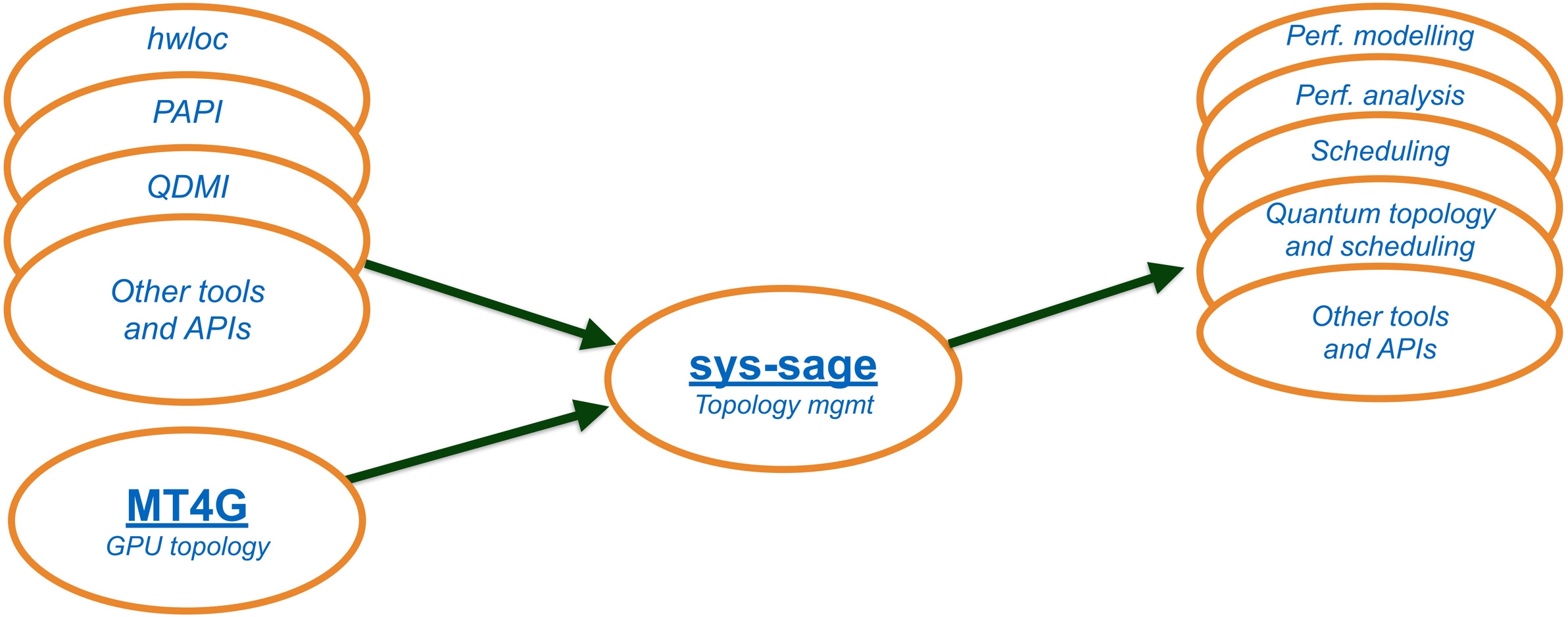

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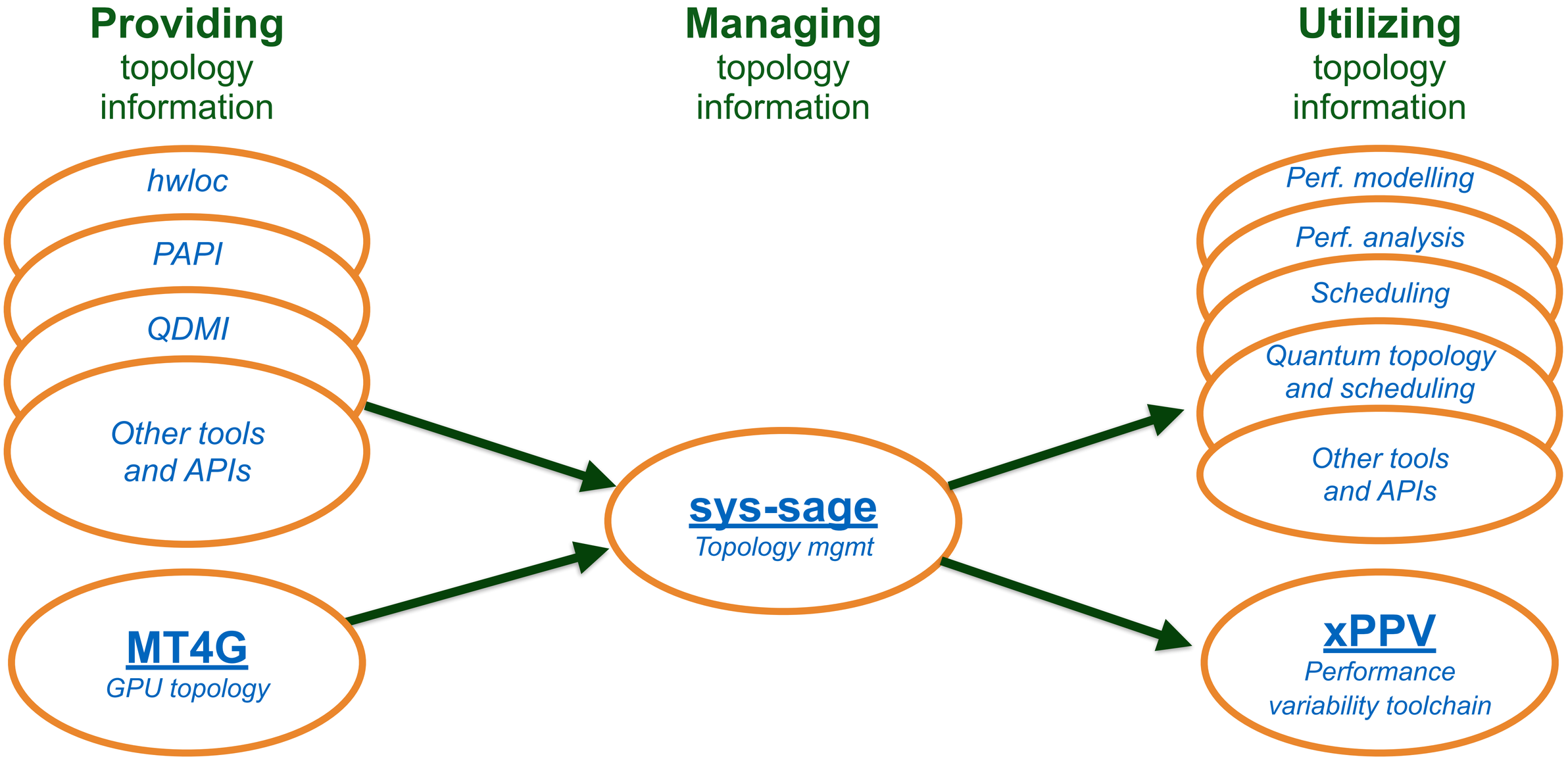

MT4G — Motivation

Vanecek, Mußbacher, Größler, Saroliya, Schulz. 2025. MT4G: A Tool for Reliable Auto-Discovery of NVIDIA and AMD GPU Compute and Memory Topologies. SC ProTools '25 https://doi.org/10.1145/3731599.3767518

MT4G — Motivation

CPUs

Tools & Interfaces for discovery:

- HWloc, LIKWID, lscpu, …

Providing valuable Information:

- Number of Cores, hyperthreading
- NUMAs, sockets, ..
- Cache hierarchy & properties (size, $lines, ..)
- Main memory (incl. sizes)

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- —lack ot standardized ones—
- nvidia-smi, rocm-smi, hipdeviceproperties, ..

Scattered information:

- nvidia-smi: GPU name, memory size
- cuda/hipdeviceprop: L2 cache size
- nvml: GPU configuration

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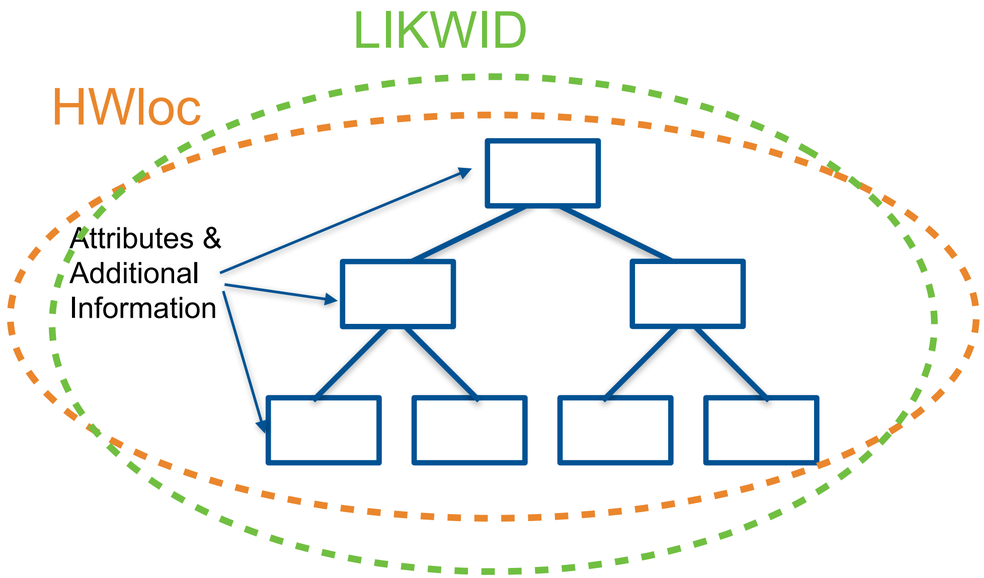
Complete, cross-vendor



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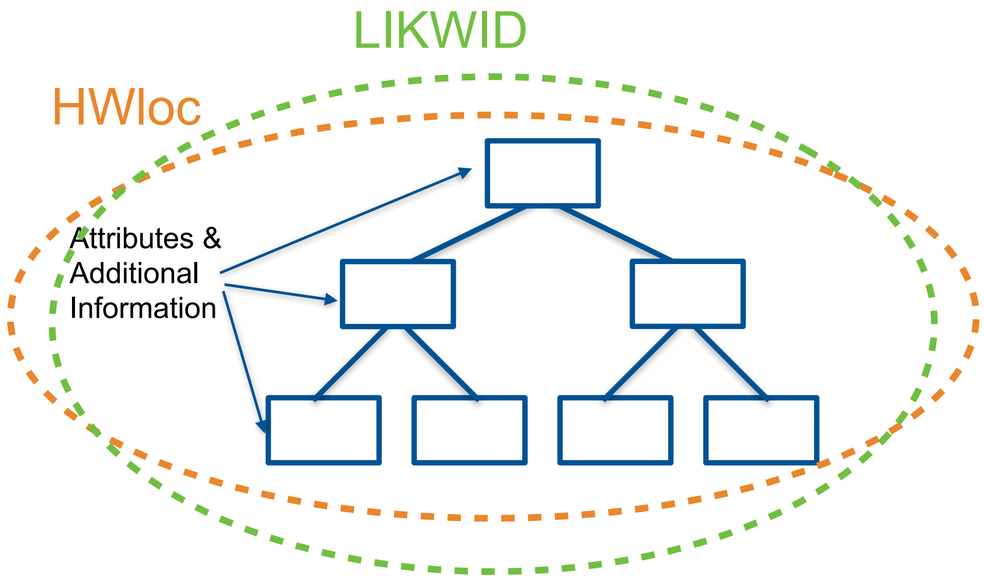

GPUs

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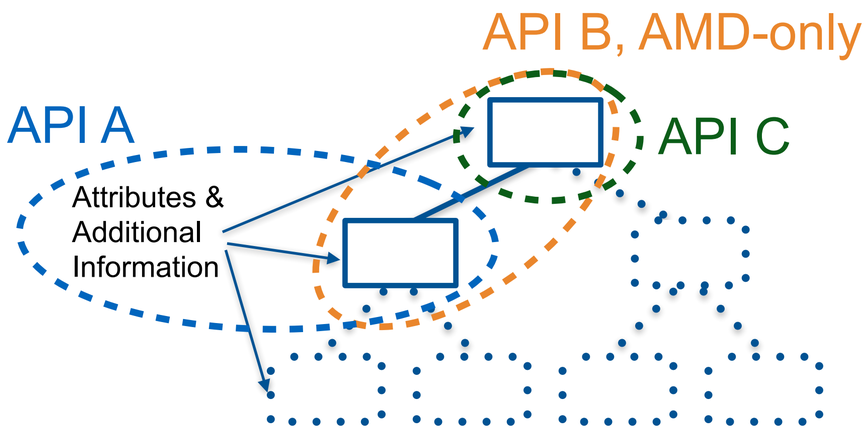

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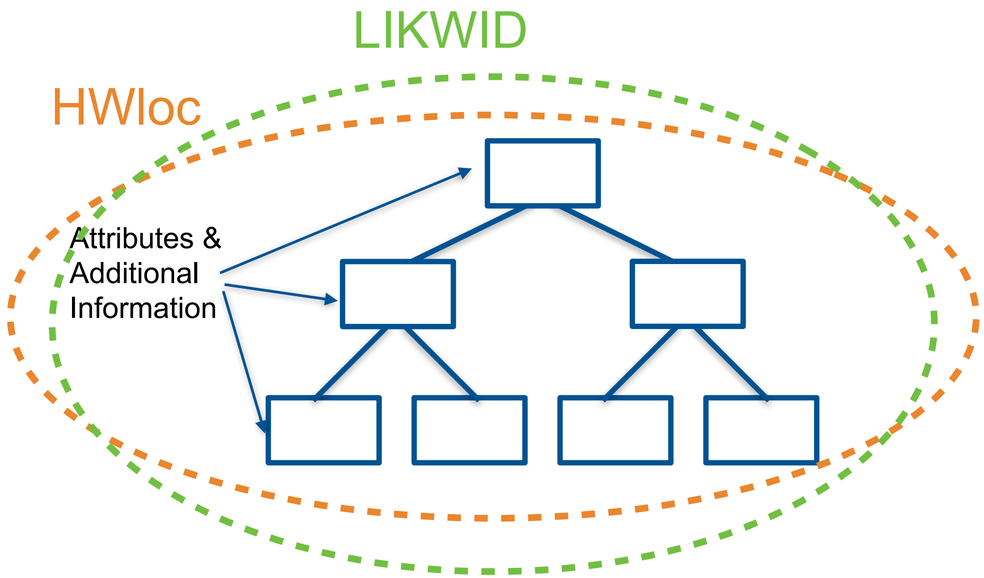

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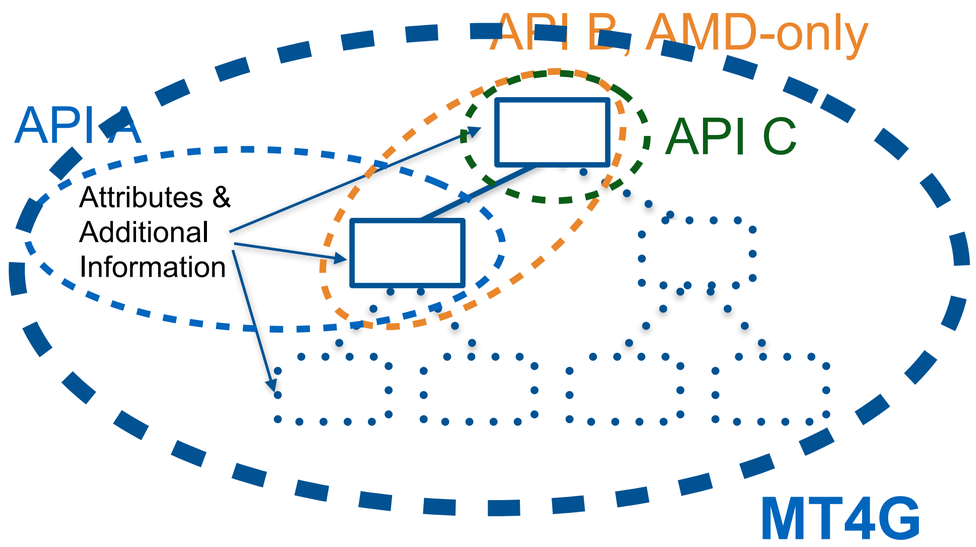

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What does MT4G provide?

Report on GPU building blocks and their attributes and capabilities

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Target Memory Elements

NVIDIA

- L1 cache
- L2 cache
- Texture & Readonly cache
- Constant L1, L1.5 cache
- Shared memory
- Device memory

AMD

- L1 cache
- L1s cache
- L2 cache
- L3 cache (partially)
- Local Data Share
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Queried properties

- Size
- Cache Line Size ($-only)
- Fetch Granularity ($-only)
- Physical Layout
- Load Latency
- Read & Write Bandwidth (L2 cache and above)

\+ Compute Resource Topological Information

MT4G — Attribute Coverage

Memory Element	Size		LD lat		R&W BW		cache line size		fetch granularity		Amount per SM/GPU		Physical hardware sharing	
Vendor	*NV*	*AMD*	*NV*	*AMD*	*NV*	*AMD*	*NV*	*AMD*	*NV*	*AMD*	*NV*	*AMD*	*NV*	*AMD*
(v) L1 cache	✅	✅	✅	✅	SOON	SOON	✅	✅	✅	✅	✅	✅	✅	
sL1 cache		✅		✅		SOON		✅		✅				✅
L2 cache	☑	☑	✅	✅	✅	✅	✅	☑	✅	✅	✅	☑		
L3 cache		☑		SOON		✅		☑		SOON		☑		
Texture cache	✅		✅		SOON		✅		✅		✅		✅	
Readonly cache	✅		✅		SOON		✅		✅		✅		✅	
Constant L1 cache	✅		✅		SOON		✅		✅		✅		✅	
Constant L1.5 cache	✅		✅		SOON		❌		✅		❌			
Shared Mem. / LDS	☑	☑	✅	✅	SOON	SOON								
Device Memory	☑	☑	✅	✅	✅	✅								

✅ = Available via microbenchmark; ☑ = Available via API; SOON = Work-in-progress; ❌ = not available

sys-sage — Motivation

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sys-sage — Motivation

? Current landscape of topological information

- Multiple tools (such as hwloc) provide static topological snapshot
- Increased need for dynamic/runtime data (interfaces also exist)
- Need to integrate multiple static and dynamic contexts ➡ manual integration

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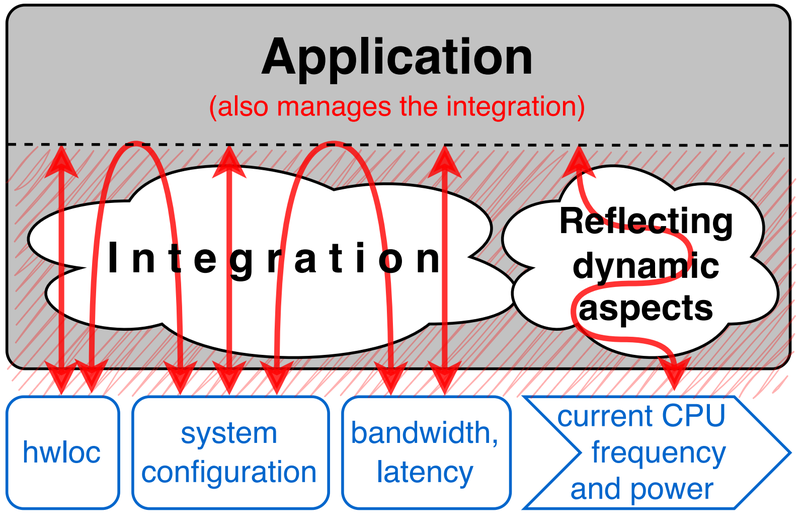
Traditional approach



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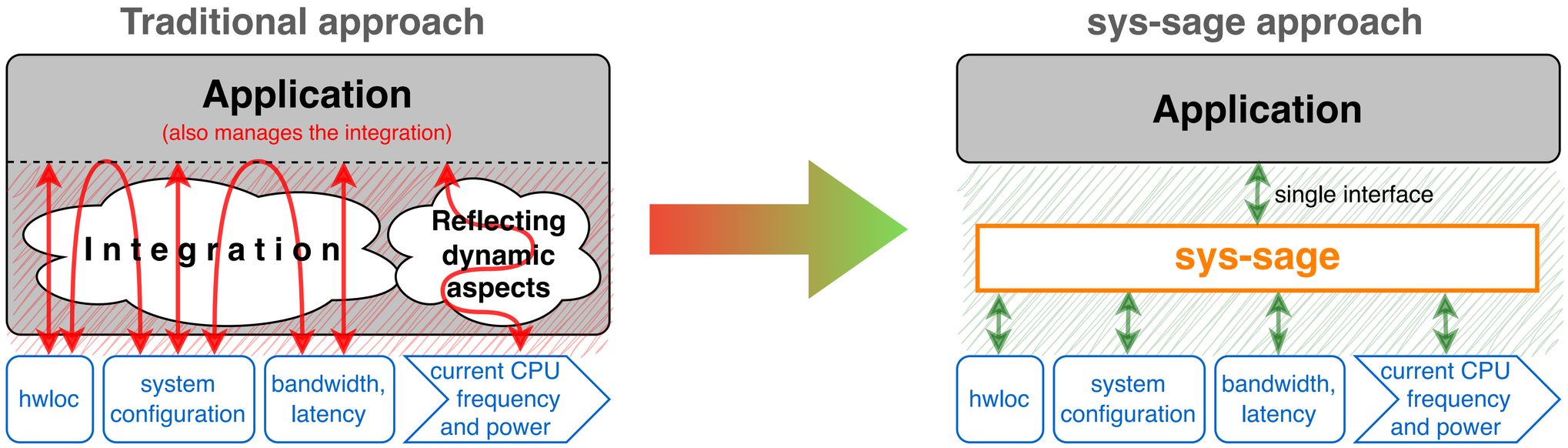

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Internal Data Representation

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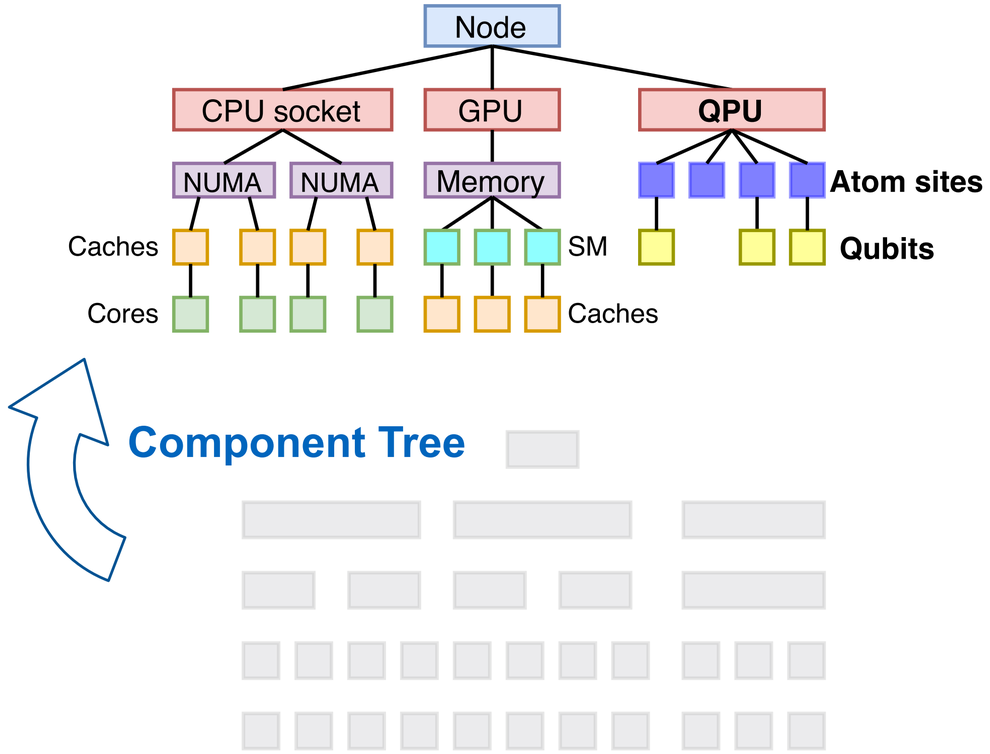
- Hierarchical representation (hwloc-like)
- Simple to understand, Mandatory
- Examples: Static CPU/GPU/QPU HW topologies



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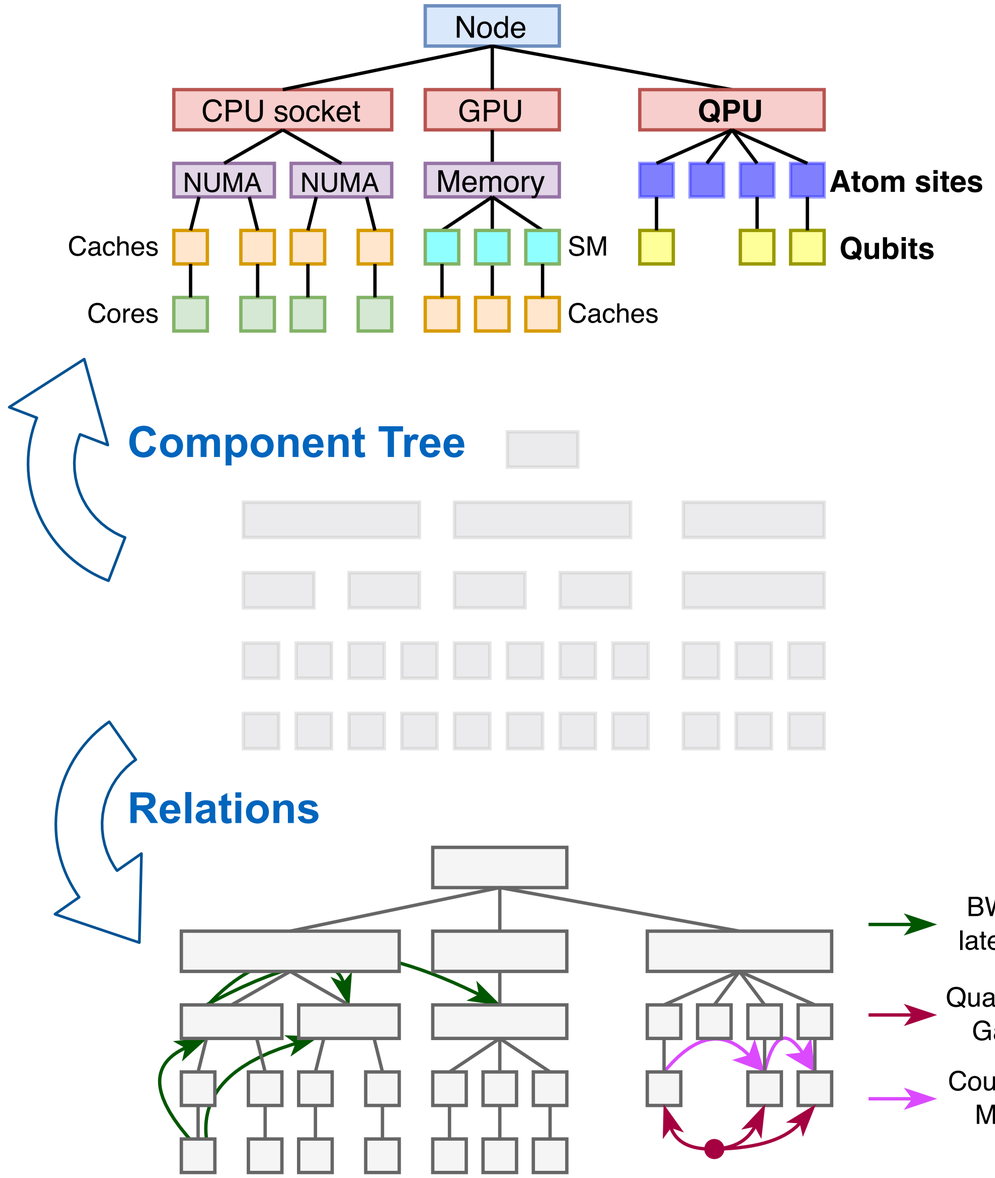
2. Relations

- Any Relation of 1 or more Components
- Orthogonal to the Component Tree
- More dynamic, complex information
- Examples: data exchange rates between components, dynamic settings, HW counter readings



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sys-sage

Quantum Extension

- Quantum Processing Units (QPUs) begin to accompany CPUs and GPUs in HPC systems
- sys-sage was extended to support QPUs alongside CPUs/GPUs
- Possible to retrieve information from existing APIs, such as QDMI or Qiskit runtime

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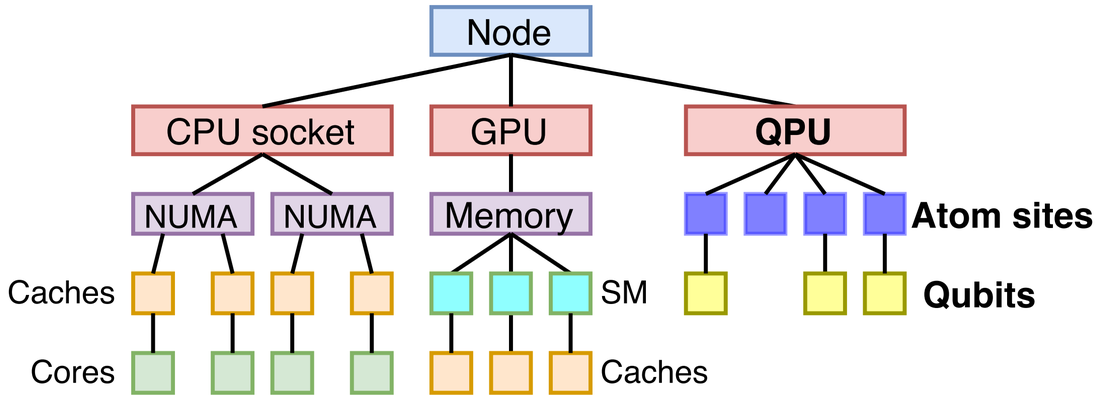

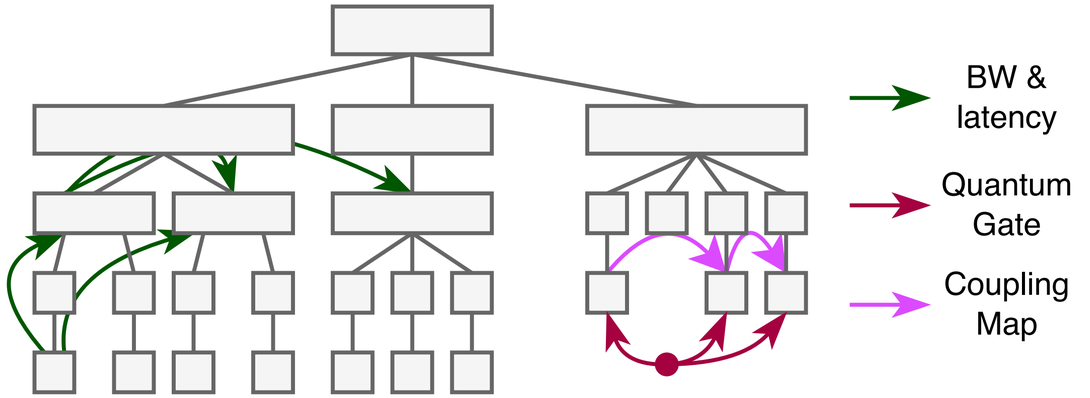

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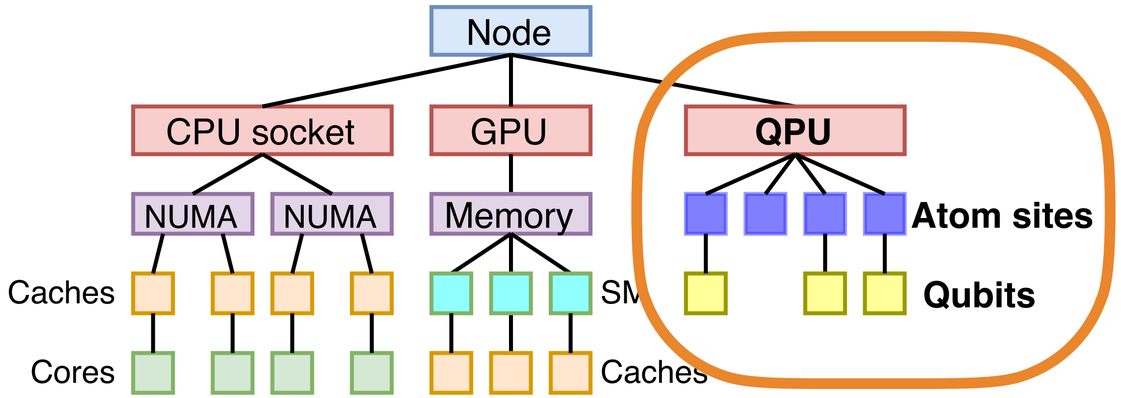

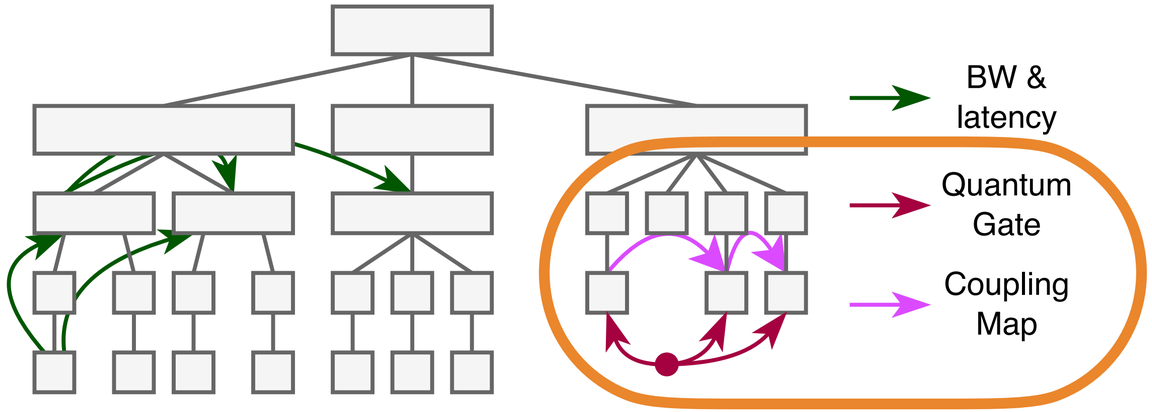

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sys-sage — Out-of-the-box integrations

Data Parsers

static information at startup

- hwloc (CPU topology)
- MT4G (GPU topology)
- IQM (quantum topology information)
- MUSA topology (simulator-based CPU topology)
- Performance benchmarks and microbenchmarks (through xPPV)
  - FIRESTARTER, BabelSTREAM, NAS Parallel Benchmarks, HPL, LULESH, cccbench

3rd Party API

dynamic information during runtime

- Intel PQOS (CPU resource isolation)
- NVIDIA MIG (GPU resource isolation)
- proc_cpuinfo (CPU frequency)
- PAPI (performance counters)
- QDMI (Quantum systems information)

xPPV — Understanding CPU Performance Variability

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HPC systems' components exhibit different performance

- *(random)* effects of manufacturing process
- *(random)* misconfiguration / HW failures
- *(systemic)* chip/node/system architecture artifacts

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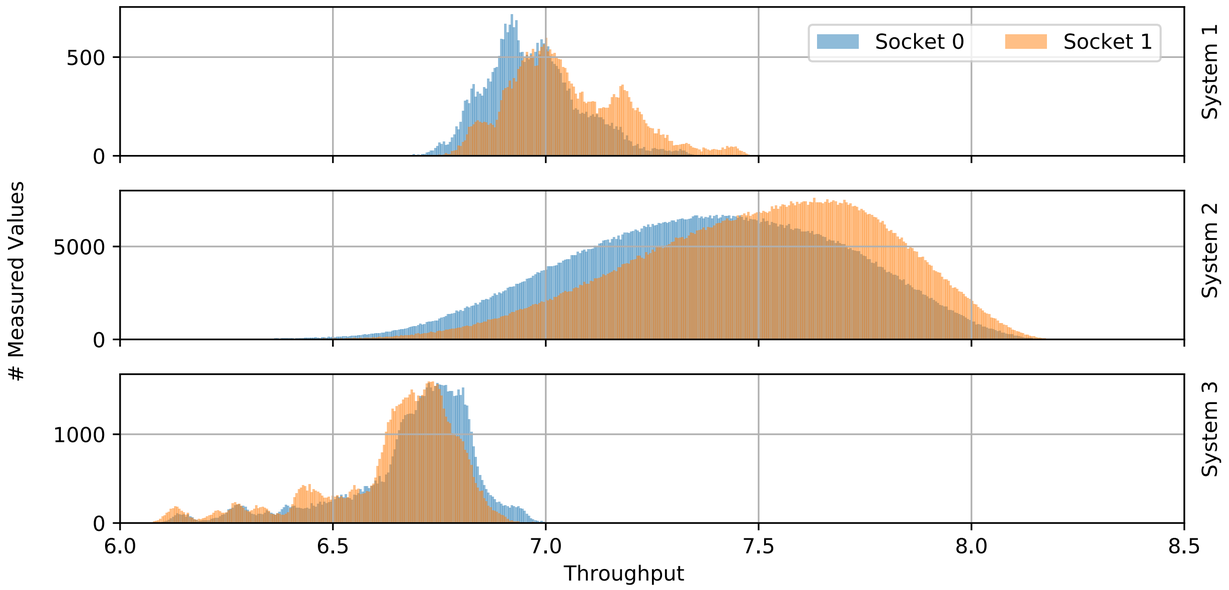

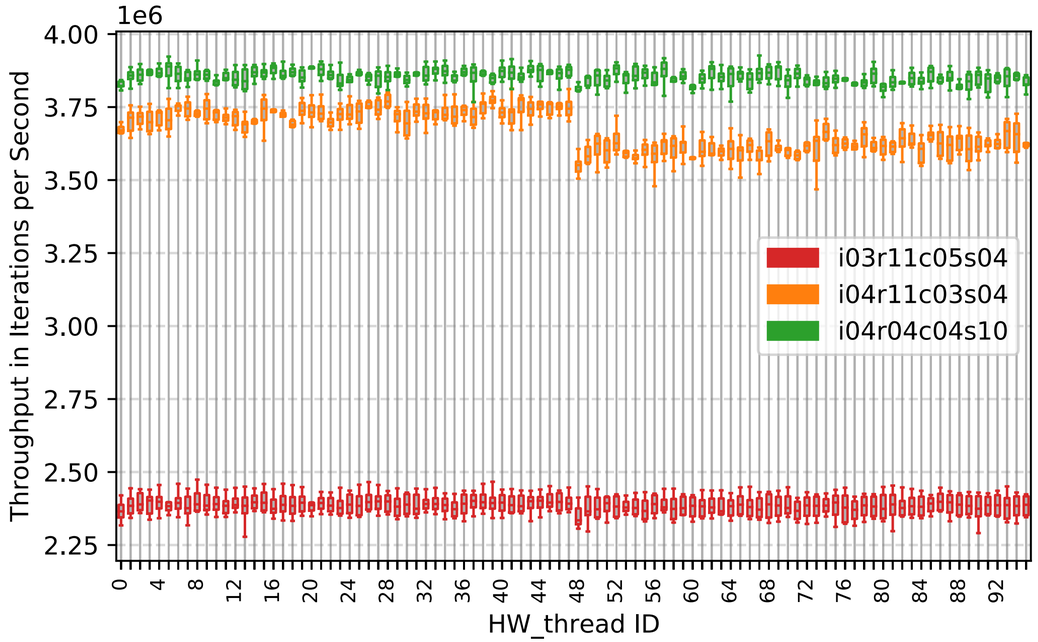

xPPV — End-to-end Toolchain

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- Runs arbitrary benchmarks on specified HW resrouces
- sys-sage topology context (hwloc)

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- An API as an extension of sys-sage
- Variability information in the topology context

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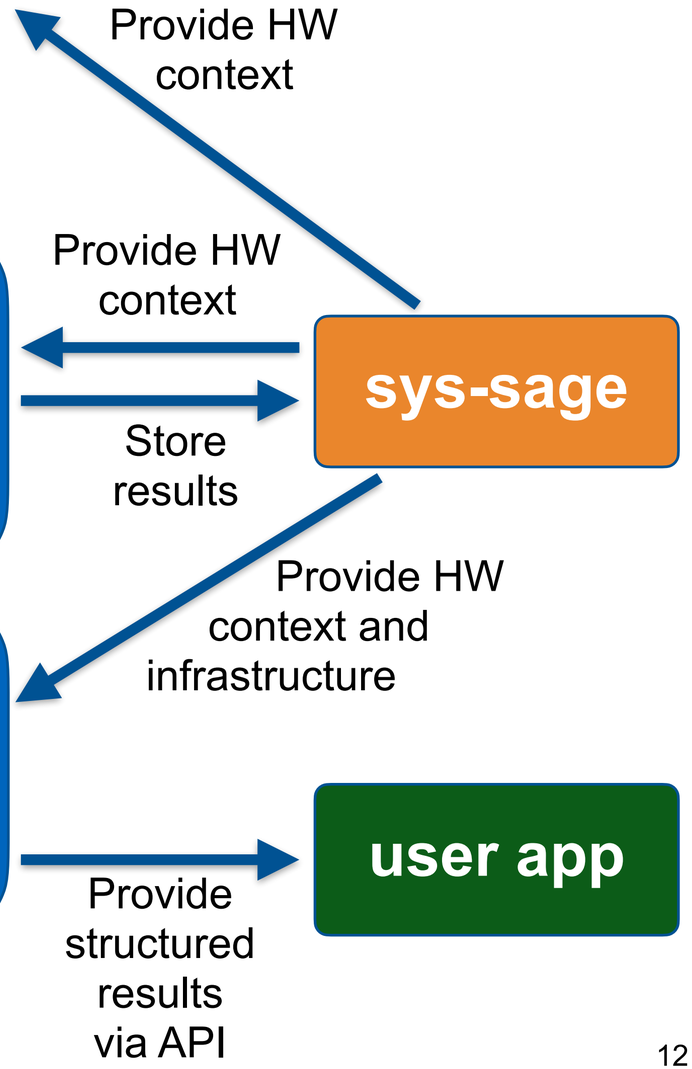

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A toolkit for collecting, managing, and utilizing topological information about HPC systems

Tools

MT4G

GitHub: https://github.com/caps-tum/mt4g

Paper ➡

sys-sage

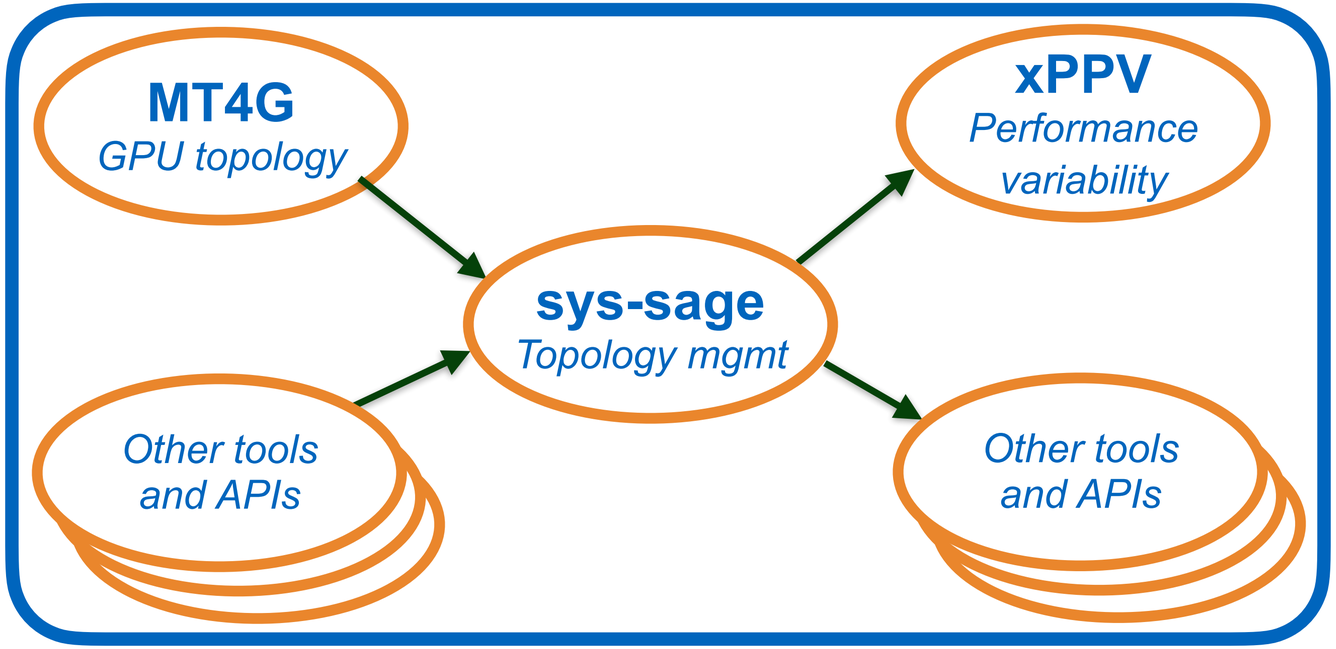
GitHub: https://github.com/caps-tum/sys-sage

⬅ Original Concept Paper

Quantum Extension Paper ➡

xPPV

Work-in-progress, not yet publicly available.
Reach out if you are interested.



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Chair of Computer Architecture and Parallel Systems (CAPS)
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