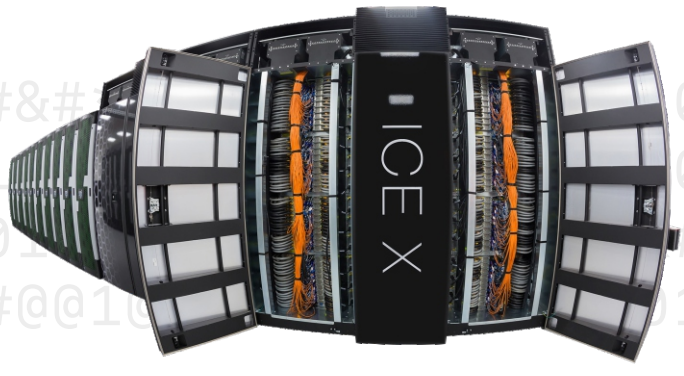
IT4Innovations national supercomputing center



INTEL MIC PROGRAMMING WORKSHOP

February 7 – 8, 2017

VŠB - Technical University Ostrava

LECTURERS

Volker Weinberg, Momme Allalen Leibniz Supercomputing Centre
Branislav Jansík IT4Innovations

The course discusses Intel's Many Integrated Core (MIC) architecture. It covers various programming and optimisation techniques for Intel Xeon Phi coprocessors. We will mainly focus on the KNC version of the chip. The hands-on sessions are done on the Intel Xeon Phi based Salomon system at the IT4Innovations National Supercomputing Center. The afternoon of the second day will be devoted to a workshop with invited talks about Intel Xeon Phi experience on Salomon.

Tuesday February 7, 2017

09:00	09:30	Registration
09:30	09:45	Welcome
09:45	10:30	Salomon intro
10:30	11:00	Coffee break
11:00	12:00	Overview of the Intel MIC architecture and programming models
12:00	13:00	Lunch break
13:00	13:30	Native mode programming
13:30	15:30	OpenMP and offloading I
15:30	16:00	Coffee break
16:00	17:00	OpenMP and offloading II

Wednesday February 8, 2017

09:00	10:30	MPI
10:30	11:00	Coffee break
11:00	12:00	Vectorisation and Intel Xeon Phi performance optimisation
12:00	13:00	Lunch break
13:00	15:30	Talks about Xeon Phi experiences on Salomon
15:30	16:00	Coffee break
16:00	17:00	Talks about Xeon Phi experiences on Salomon

More information and registration
https://events.prace-ri.eu/event/583/